Fraunhofer IIS

CAN I COMBINE SCIENCE AND BUSINESS IN A SINGLE JOB?

YES.

We´ll show you how at Fraunhofer IIS.

For the **Broadband & Broadcast** department in **Erlangen**, the Fraunhofer Institute for Integrated Circuits IIS is currently seeking

Master Thesis Students for the topic: Design of efficient Neuromorphic Hardware Architectures

The Broadband & Broadcast (BB) department is active in the areas of mobile communications, satellite communications, Internet-of-Things and automotive communication systems. We take new concepts and algorithms in the fields of communications and digital signal processing (e.g. machine learning) from theory, implement them and test them in simulations and in prototypes in our labs and in the field.

Abstract:

Neuromorphic hardware is a brand new type of integrated circuits which are used to accelerate significantly the calculation of Deep Neural Networks (DNN), thus reducing power consumption, latency and cost. Due to the very high numerical complexity of DNNs, efficient hardware implementations of neural network architectures are the key to widespread deployment in embedded devices for inference tasks. Research in this domain is ongoing and first promising concepts like so-called Deep Compression have been devised. This thesis focuses on study and development of novel efficient neural network architectures in digital hardware and their implementation and evaluation on FPGA-based platforms.

Your responsibilities:

- Analysis of state-of-the-art approaches for efficient implementation of neural networks (e.g. Deep Compression)
- Development of new approaches for efficient neural network architectures and implement them on FPGA-based platforms
- Analysis and comparison of different neural network architectures with respect to hardware performance indicators (e.g. throughput, hardware resources, power)

Your profile: You …

- have basic knowledge of digital hardware design using VHDL or System Verilog (mandatory)
- have an understanding of Deep Neural Network models (mandatory)
- ideally have practical experience with FPGA platforms (e.g. Xilinx Zynq)

What you can expect from us

- An open and cooperative working environment
- Collaboration in interesting and innovative projects
- Many opportunities to gain practical experience

The thesis will be assigned and carried out in accordance with the rules of your university. For this reason, please discuss the thesis with a professor who can advise you over the course of the project.
The duration for the thesis should be 6 months and it can be started from now on.

Interested?

Please apply for this position via the following link:
https://recruiting.fraunhofer.de/Vacancies/39386/Description/2

Please address your full application (in PDF, including a cover letter, CV, latest transcripts of records, references and the date of your earliest possible start date) to Nina Wörlein, quoting ID number **39386-BBT-042et.**
Please let us know how you became aware of this position.

Additional information is available on our website: www.iis.fraunhofer.de/en